EXHIBIT 13

Electronically filed April 10, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee et al.	Confirmation No.:	3694
Serial No.:	16/391,151	Art Unit:	2183
Filed:	April 22, 2019	Examiner:	Sun, Michael
For:	*MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING*	Attorney Docket No.:	129980-5049-US01

RESPONSE TO OFFICE ACTION

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment is in response to the Office Action dated January 10, 2020 for the above identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5049-US01).

Electronic Acknowledgement Receipt

EFS ID:	39130538
Application Number:	16391151
International Application Number:	
Confirmation Number:	3694
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5049-US01
Receipt Date:	10-APR-2020
Filing Date:	22-APR-2019
Time Stamp:	18:25:08
Application Type:	Utility under 35 USC 111(a)

Payment information:

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980-5049US01_AMEND.pdf	177364 7ce7cf2b5614a88c12c2a72ef8f13338874f7f48	yes	13

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Applicant Arguments/Remarks Made in an Amendment	10	13
Claims	2	9
Amendment/Req. Reconsideration-After Non-Final Reject	1	1

Warnings:	
Information:	
Total Files Size (in bytes):	177364

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS

This amendment responds to the office action mailed January 1●, 2●2●. In the office action, the Examiner:

- rejected claim 1 on the ground of nonstatutory double patenting over claims 1-12 of copending Application No. 15/82●,●76, now U.S. Patent No. 10,268,6●8;
- rejected claim 1 on the ground of nonstatutory double patenting over claims 1-22 of copending Application No. 15/426,●64, now U.S. Patent No. 9,824,●35;
- rejected claim 1 on the ground of nonstatutory double patenting over claims 1-2● of copending Application No. 14/846,993, now U.S. Patent No. 9,563,587;
- rejected claim 1 on the ground of nonstatutory double patenting over claims 1-2● of copending Application No. 13/952,599, now U.S. Patent No. 9,128,632; and
- rejected claim 1 as being anticipated by Manohararajah et al. (US 8,565,●33).

REMARKS CONCERNING CLAIMS

Claim 1 has been canceled.

Claims 2-21 have been added.

Support for the amendments can be found in at least paragraphs [●●34], [●●47], [●●5●], [●●52], [●●61]-[●●74], and [●●83]-[●●97], and the Figures referenced to in these paragraphs of the application as filed. No new matter has been added.

With respect to all amendments, Applicant has not dedicated or abandoned any unclaimed subject matter. Moreover, Applicant has not acquiesced to any characterizations of the invention, nor any rejections or objections of the claims, made by the Examiner. Moreover, the Applicant hereby rescinds any prior disclaimer of claim scope, to the extent they exist, made during the prosecution of this application or made during the prosecution of any patent or other related patents/applications, and advises the Examiner that any such previous disclaimers and the cited references that they were made to avoid may need to be revisited.

After entry of this amendment, the pending claims are: claims 2 - 21.

REMARKS CONCERNING DOUBLE PATENTING REJECTIONS

I. REJECTION OF CLAIM 1 ON THE GROUND OF NONSTATUTORY DOUBLE PATENTING OVER CLAIMS 1-12 OF COPENDING APPLICATION NO. 15/820,076, NOW U.S. PATENT NO. 10,268,608

A terminal disclaimer is being filed concurrently with this response to address this nonstatutory double patenting rejection.

Applicant respectfully requests that these rejections be withdrawn.

II. REJECTION OF CLAIM 1 ON THE GROUND OF NONSTATUTORY DOUBLE PATENTING OVER CLAIMS 1-22 OF COPENDING APPLICATION NO. 15/426,064, NOW U.S. PATENT NO. 9,824,035

A terminal disclaimer is being filed concurrently with this response to address this nonstatutory double patenting rejection.

Applicant respectfully requests that these rejections be withdrawn.

III. REJECTION OF CLAIM 1 ON THE GROUND OF NONSTATUTORY DOUBLE PATENTING OVER CLAIMS 1-20 OF COPENDING APPLICATION NO. 14/846,993, NOW U.S. PATENT NO. 9,563,587

A terminal disclaimer is being filed concurrently with this response to address this nonstatutory double patenting rejection.

Applicant respectfully requests that these rejections be withdrawn.

IV. REJECTION OF CLAIM 1 ON THE GROUND OF NONSTATUTORY DOUBLE PATENTING OVER CLAIMS 1-20 OF COPENDING APPLICATION NO. 13/952,599, NOW U.S. PATENT NO. 9,128,632

A terminal disclaimer is being filed concurrently with this response to address this nonstatutory double patenting rejection.

Applicant respectfully requests that these rejections be withdrawn.

REMARKS CONCERNING REJECTIONS UNDER 35 U.S.C. 102

V. REJECTION OF CLAIM 1 AS BEING ANTICIPATED BY MANOHARARAJAH

Claim 1 has been cancelled. New claims 2-21 are patentable over Manohararajah.

With respect to claim 2, Manohararajah does not disclose or teach all of the elements arranged as claimed. For example, claim 2 recites:

> "a module control device on the module board configurable to ***receive*** input C/A signals corresponding to a memory read operation via the C/A signal lines and to output registered C/A signals in response to the input C/A signals and to output module control signals."
>
> *Emphasis added.*

Manohararajah does not teach a memory module including such a module control device. In Manohararajah, the memory module 22 is shown to includes memory groups 52-1 to 52-N but no module control device. The memory interface circuitry 24 in Manohararajah, which is on the other side of the buses 34/36, ***outputs*** instead of ***receiving*** input C/A signals corresponding to a memory read operation via the C/A signal lines. Therefore, the memory interface circuitry 24 in Manohararajah cannot be likened to the module control device in claim 2.

As another example, claim 2 further recites:

> "a module board having edge connections to be coupled to respective signal lines in the memory bus" and "data buffers on the module board and coupled ***between*** the edge connections and the memory devices."
>
> *Emphasis added.*

Again, Manohararajah does not teach these claimed features. In Manohararajah, the I/O circuit 54, read-sync buffers 60, and read-valid buffers 62, which the Office Action refers to when discussing data buffers, are not coupled between the memory device groups 52-1 to 52-N and any edge connections to be coupled to buses 34/36. Instead, the memory device groups 52-1 to 52-3 are shown in FIGS. 4-5 as coupled directed to one side of the buses 34/36 and the I/O circuit 54, read-sync buffers 60, and read-valid buffers 62 are on the other side of the buses 34/36. Thus, Manohararajah does not disclose or teach "data buffers on the module board and coupled ***between*** the edge connections and the memory devices," as recited in claim 2.

As a further example, claim 2 further recites:

> "a first data buffer of the data buffers is coupled to the first memory device and is configurable to, in response to the module control signals, … ***transmit*** the first section of the read data to a first section of the data bus."
>
> *Emphasis added.*

In contract, the I/O circuit 54, read-sync buffers 60, and read-valid buffers 62 in Manohararajah ***receive*** read data and read strobes from bus 34 instead of transmitting read data and read strobe to bus 34.

Therefore, Manohararajah does not teach each and every element of claim 2, and claim 2 is patentable over Manohararajah.

Claims 3-14 depend from claim 2 and include further limitations in addition to the limitation in claim 2. Therefore, claims 3-14 are patentable for at least the same reasons claim 2 is patentable.

The arguments regarding claim 2 apply to claim 15. Therefore, claim 15 is also patentable over Manohararajah.

Claims 16-21 depend from claim 15 and include further limitations in addition to the limitation in claim 15. Therefore, claims 16-21 are patentable for at least the same reasons claim 15 is patentable.

CONCLUDING REMARKS

By responding in the foregoing remarks only to particular positions asserted by the examiner, the Applicant does not necessarily acquiesce in other positions that have not been explicitly addressed. In addition, the Applicant's arguments for the patentability of a claim should not be understood as implying that no other reasons for the patentability of that claim exist.

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 843-4000, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: April 10, 2020

/Jamie J. Zheng/ 51,167

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Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)

2. (New) A memory module operable in a computer system to communicate with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module comprising:

a module board having edge connections to be coupled to respective signal lines in the memory bus;

a module control device on the module board configurable to receive input C/A signals corresponding to a memory read operation via the C/A signal lines and to output registered C/A signals in response to the input C/A signals and to output module control signals;

memory devices arranged in multiple ranks on the module board and coupled to the module control device via module C/A signal lines that conduct the registered C/A signals, wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is configurable to output at least a first section of the read data and at least a first read strobe; and

data buffers on the module board and coupled between the edge connections and the memory devices, wherein a respective data buffer of the data buffers is coupled to at least one respective memory device in each of the multiple ranks and is configurable to receive the module control signals from the module control device, and wherein a first data buffer of the data buffers is coupled to the first memory device and is configurable to, in response to one or more of the module control signals:

delay the first read strobe by a first predetermined amount to generate a first delayed read strobe;

sample the first section of the read data using the first delayed read strobe; and

transmit the first section of the read data to a first section of the data bus;

wherein the first predetermined amount is determined based at least on signals received by the first data buffer before the memory read operation.

3. (New) The memory module of claim 2, wherein a second memory device in the selected rank is configurable to output at least a second section of the read data and at least a second read strobe, and wherein the data buffers further include a second data buffer configurable to, in response to the one or more of the module control signals:

delay the second read strobe by a second predetermined amount to generate a second delayed read strobe;

sample the second section of the read data using the second delayed read strobe; and

transmit the second section of the read data to a second section of the data bus;

wherein the second predetermined amount is determined based at least on signals received by the second data buffer before the memory read operation.

4. (New) The memory module of claim 3, wherein a third memory device in the selected rank is configurable to output a third section of the read data and a third read strobe, wherein each of the first section, the second section, and the third section of the read data is 4-bit wide, and wherein the first data buffer is further coupled to the third memory device and is further configurable to, in response to the one or more of the module control signals:

delay the third read strobe by a third predetermined amount to generate a third delayed read strobe;

sample the third section of the read data using the third delayed read strobe concurrently with sampling the first section of the read data using the first delayed read strobe; and

transmit the third section of the read data to a third section of the data bus concurrently with transmitting the first section of the read data to the first section of the data bus;

wherein the third predetermined amount is determined based at least on signals received by the first data buffer before the memory read operation.

5. (New) The memory module of claim 3, wherein the signals received by the first data buffer before the memory read operation includes at least a strobe signal associated with a previous operation, and wherein the signals received by the second data buffer before the

memory read operation includes at least another strobe signal associated with the previous operation.

6. (New) The memory module claim 3, wherein each of the first section and the second section of the read data is 4-bit wide, and wherein the at least one respective memory device in each of the multiple ranks includes one memory device having a bit width of 8 or two memory devices each having a bit width of 4.

7. (New) The memory module of claim 2, wherein the signals received by the first data buffer before the memory read operation includes at least a strobe signal associated with a previous operation.

8. (New) The memory module of claim 2, wherein the module control device is further configurable to receive a system clock signal and output a module clock signal, and wherein the first data buffer is further configurable to:

receive the module clock signal;

generate a local clock signal having a programmable phase relationship with the module clock signal; and

output the local clock signal;

wherein the first memory device is configurable to receive the local clock signal and to output the first section of the read data and first read strobe in accordance with the local clock signal.

9. (New) The memory module of claim 2, wherein the module control device is further configurable to receive a system clock signal and output a module clock signal together with the module control signals to the data buffers, and wherein the first data buffer further includes receiver circuits corresponding to respective ones of the module control signals, a respective receiver circuit for a respective module control signal including a metastability detection circuit configurable to generate one or more metastability indicators indicating a metastability condition in the respective module control signals with respect to the module clock signal.

10. (New) The memory module of claim 9, wherein the metastability detection circuit is further configurable to generate at least one delayed version of the module clock signal, and at least one delayed version of the respective module control signal, and wherein the respective receiver circuit further includes a signal selection circuit configurable to receive the module clock signal and the at least one delayed version of the module clock signal, and to select a clock signal from among the module clock signal and the at least one delayed version of the module clock signal based on at least a first metastability indicator of the one or more metastability indicators.

11. (New) The memory module of claim 10, wherein the signal selection circuit is further configurable to receive the respective module control signal and the at least one delayed version of the respective module control signal, and to select a module control signal from among the respective module control signal and the at least one delayed version of the respective module control signal based at least on a second metastability indicator of the one or more metastability indicators; and wherein the respective receiver circuit further includes a sampler that samples a selected module control signal according to a selected module clock signal and outputs received respective module control signal.

12. (New) The memory module of claim 2, wherein the first data buffer includes circuitry that determines the first predetermined amount based at least on the signals received by the first data buffer before the memory read operation.

13. (New) The memory module of claim 2, wherein the first section of the read data is 4-bit wide, and wherein the at least one respective memory device in each of the multiple ranks includes one memory device having a bit width of 8 or two memory devices each having a bit width of 4.

14. (New) The memory module of claim 2, wherein the memory devices are selected from the group consisting of dynamic random-access memory, synchronous dynamic random-access memory, and double-data-rate dynamic random-access memory.

15. (New) A method, comprising:

at a memory module in a computer system and operable to communicate data with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module including a module board having edge connections to be coupled to respective signal lines in the memory bus, a module control device on the module board, memory devices arranged in multiple ranks on the module board and coupled to the module control device, and data buffers on the module board and coupled between the edge connections and the memory devices, the data buffers including a first data buffer, wherein each respective data buffer is coupled to one respective memory device having a bit width of 8 or two respective memory devices each having a bit width of 4 in each of the multiple ranks;

receiving, at the module control device, input C/A signals corresponding to a memory read operation via the C/A signal lines;

outputting, at the module control device, registered C/A signals in response to the input C/A signals, wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is coupled to the first data buffer and is configurable to output at least a first section of the read data and at least a first read strobe;

outputting, at the module control device, module control signals;

receiving, at each of the data buffers, the module control signals from the module control device;

the method further comprising, at the first data buffer, in response to one of more of the module control signals:

delaying the first read strobe by a first predetermined amount to generate a first delayed read strobe;

sampling the first section of the read data using the first delayed read strobe; and

transmitting the first section of the read data to a first section of the data bus; and

the method further comprising, before receiving the input C/A signals corresponding to the memory read operation at the module control device, determining the first predetermined amount based at least on signals received by the first data buffer.

16. (New) The method of claim 15, wherein the data buffers further include a second data buffer, and wherein a second memory device in the selected rank is coupled to the second data buffer and is configurable to output at least a second section of the read data and at least a second read strobe, the method further comprising, at the second data buffer, in response to the one or more of the module control signals:

delaying the second read strobe by a second predetermined amount to generate a second delayed read strobe;

sampling the second section of the read data using the second delayed read strobe; and

transmitting the second section of the read data to a second section of the data bus;

wherein the second predetermined amount is determined based on signals received by the second data buffer before the memory read operation.

17. (New) The method of claim 16, wherein a third memory device in the selected rank is coupled to the first data buffer and is configurable to output a third section of the read data and a third read strobe, the method further comprising, at the first data buffer, in response to the one or more of the module control signals:

delaying the third read strobe by a third predetermined amount to generate a third delayed read strobe;

sampling the third section of the read data using the third delayed read strobe concurrently with receiving the first section of the read data using the first delayed read strobe; and

transmitting the third section of the read data to a third section of the data bus concurrently with transmitting the first section of the read data to the first section of the data bus;

wherein the third predetermined amount is determined based on the signals received by the first data buffer before the memory read operation.

18. (New) The method of claim 16, wherein the signals received by the first data buffer before the memory read operation includes at least a strobe signal associated with a previous operation, and the signals received by the second data buffer before the memory read operation includes at least another strobe signal associated with the previous operation.

19. (New) The method of claim 15, further comprising:

receiving, at the module control device, a system clock signal concurrently with receiving the input C/A signals;

outputting, at the module control device, a module clock signal concurrently with outputting the module control signal;

receiving, at the first data buffer, the module clock signal;

generating, at the first data buffer, a local clock signal having a programmable phase relationship with the module clock signal; and

outputting, at the first data buffer, the local clock signal;

receiving, at the first memory device, the local clock signal; and

outputting, at the first memory device, the first section of the read data and first read strobe in accordance with the local clock signal.

20. (New) The method of claim 15, further comprising:

receiving, at the module control device, a system clock signal concurrently with receiving the input control and address signal;

outputting, at the module control device, a module clock signal concurrently with outputting the module control signal;

generating, at the first data buffer, one or more metastability indicators indicating a metastability condition in a respective module control signal of the module control signals with respect to the module clock signal.

21. (New) The method of claim 20, further comprising, at the first data buffer:

generating at least one delayed version of the module clock signal, and at least one delayed version of the respective module control signal;

selecting a clock signal from among the module clock signal and the at least one delayed version of the module clock signal based on at least one of the metastability indicators;

selecting a module control signal from among the respective module control signal and the at least one delayed version of the respective module control signal based at least on another metastability indicator; and

sampling the selected module control signal according to the selected module clock signal to output received respective module control signal.

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Document Description: Electronic Terminal Disclaimer - Filed

PTO/SB/26
U.S. Patent and Trademark Office
Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT**
Application Number	16391151
Filing Date	22-Apr-2019
First Named Inventor	Hyun Lee
Attorney Docket Number	129980-5049-US01
Title of Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
Netlist, Inc.	100%

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as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:
- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

(●) Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.

( ) I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.

Applicant claims the following fee status:

( ) Small Entity

( ) Micro Entity

(●) Regular Undiscounted

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

(●) An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application

Registration Number 51167

( ) A sole inventor

( ) A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application

( ) A joint inventor; all of whom are signing this request

Signature	/Jamie J. Zheng/
Name	Jamie J. Zheng

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal

Application Number:	16391151
Filing Date:	22-Apr-2019
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng/S. Olivier
Attorney Docket Number:	129980-5049-US01

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	1814	1	160	160
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**160**

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Application No.: 16391151

Filing Date: 22-Apr-2019

Applicant/Patent under Reexamination: Lee

Electronic Terminal Disclaimer filed on April 10, 2020

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt

EFS ID:	39126263
Application Number:	16391151
International Application Number:	
Confirmation Number:	3694
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5049-US01
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Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$160
RAM confirmation Number	E202040I30444621
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Terminal Disclaimer-Filed (Electronic)	eTerminal-Disclaimer.pdf	34941 44159a3c60102b2f57ccaa9e136a9465613c a557	no	3
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30632 bf60b5196fd414426c50c6a2010a8a9169ac 3ea5	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	65573		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/391,151	Filing Date 04/22/2019	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	04/10/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0		x $460 =	0
	☑ Application Size Fee (37 CFR 1.16(s))							400
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	400

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/ROSS W BROWN/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
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INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
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☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	04/10/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

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** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/ROSS W BROWN/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
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